

Fig.1

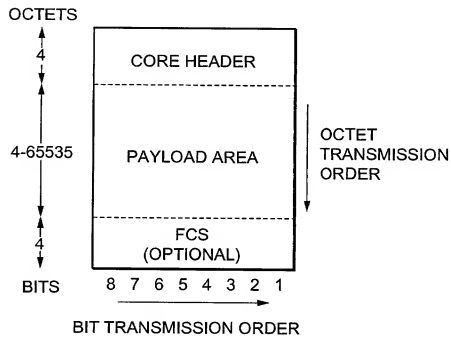


Fig.2

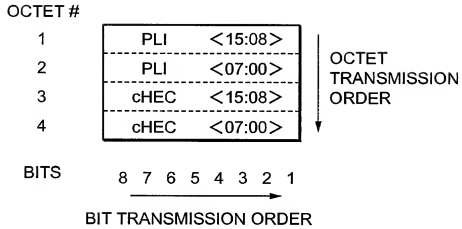


Fig.3

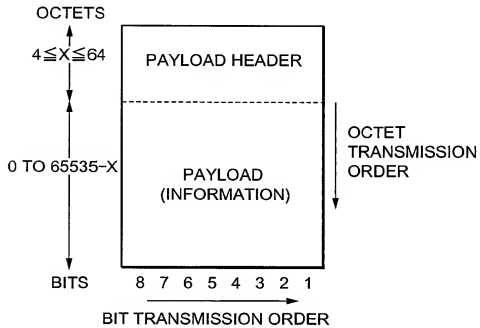


Fig.4

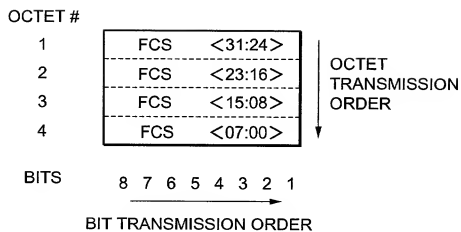


Fig.5

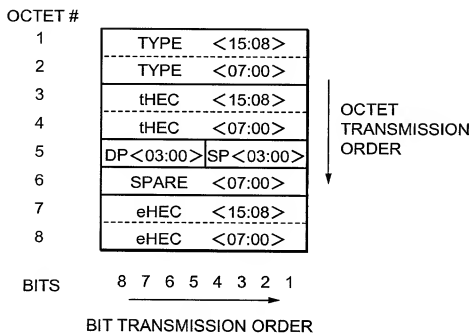


Fig.6

OCTET #

1	TYPE	<15:08>
2	TYPE	<07:00>
3	tHEC	<15:08>
4	tHEC	<07:00>
5	DP<03:00>	SP<03:00>
6	SPARE	<07:00>
7	SPARE<03:00>	DE<03:00>
8	TTL	<07:00>
9	DST MAC	<47:40>
10	DST MAC	<39:32>
11	DST MAC	<31:24>
12	DST MAC	<23:16>
13	DST MAC	<15:08>
14	DST MAC	<07:00>
15	SRC MAC	<47:40>
16	SRC MAC	<39:32>
17	SRC MAC	<31:24>
18	SRC MAC	<23:16>
19	SRC MAC	<15:08>
20	SRC MAC	<07:00>
21	eHEC	<15:08>
22	eHEC	<07:00>

OCTET
TRANSMISSION
ORDER

BITS

8 7 6 5 4 3 2 1

BIT TRANSMISSION ORDER

Fig.7

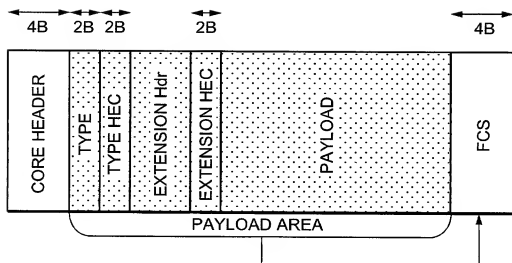


Fig.8

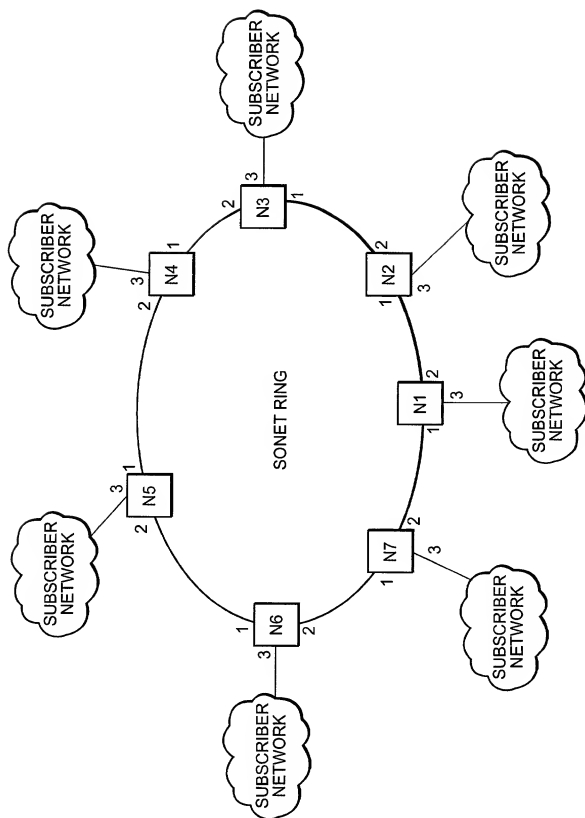


Fig.9

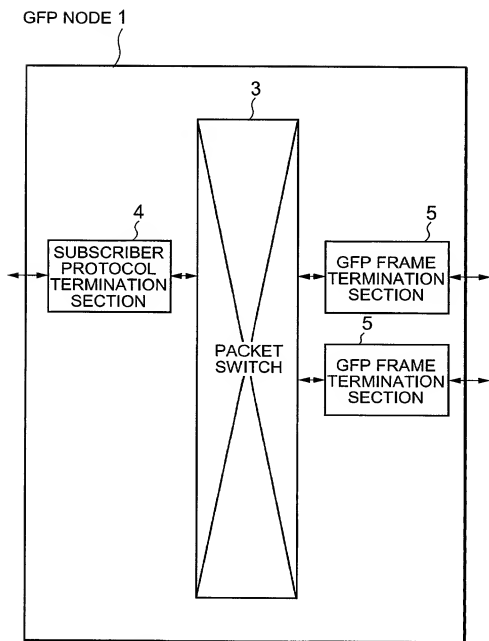


Fig.10

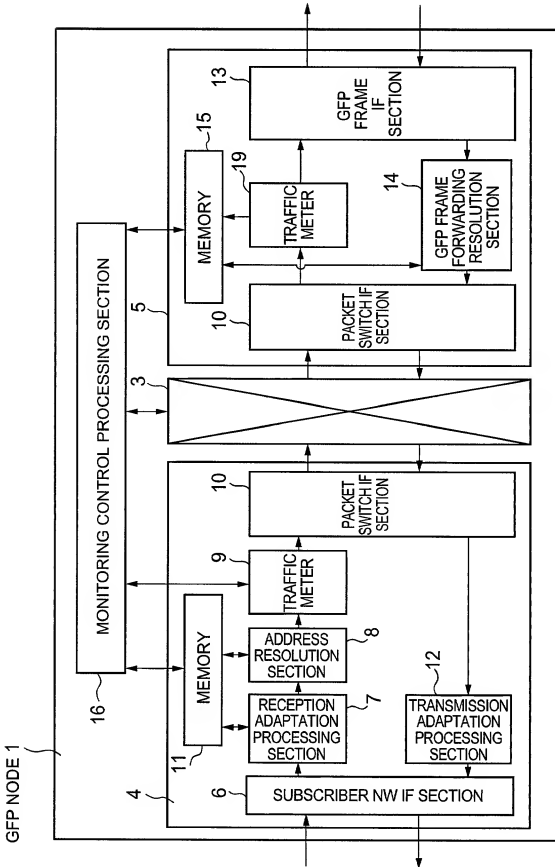


Fig.11

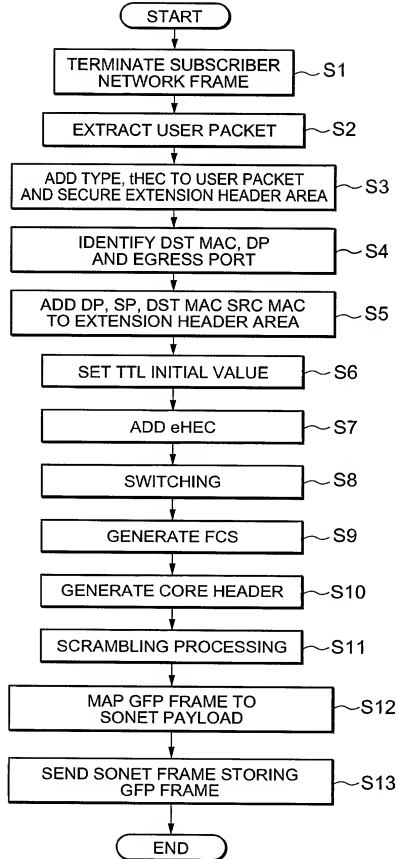


Fig.12

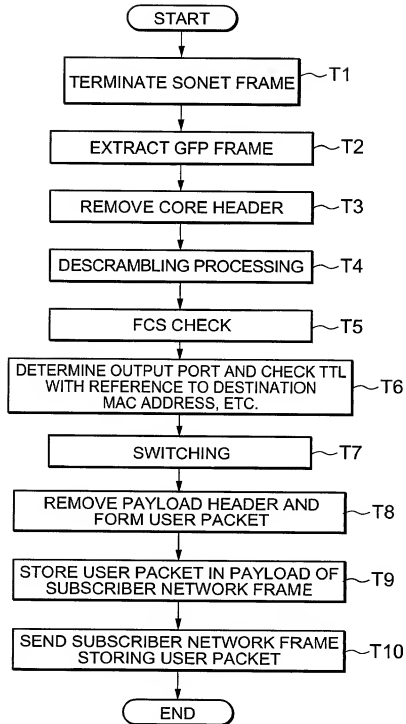


Fig.13

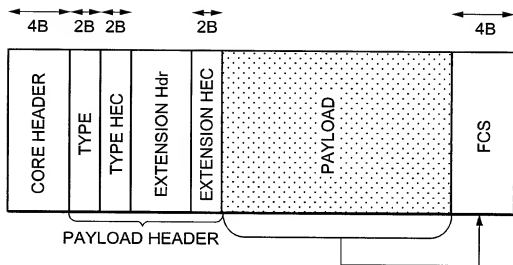


Fig.14

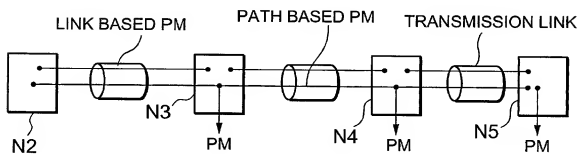


Fig.15

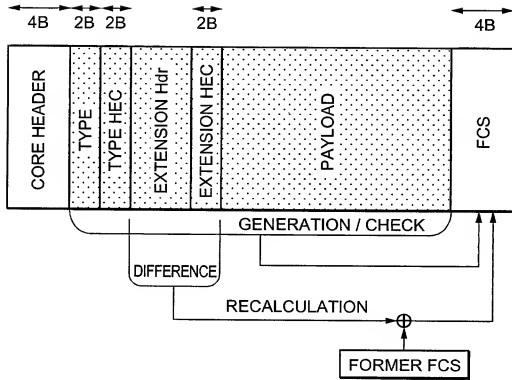


Fig.16

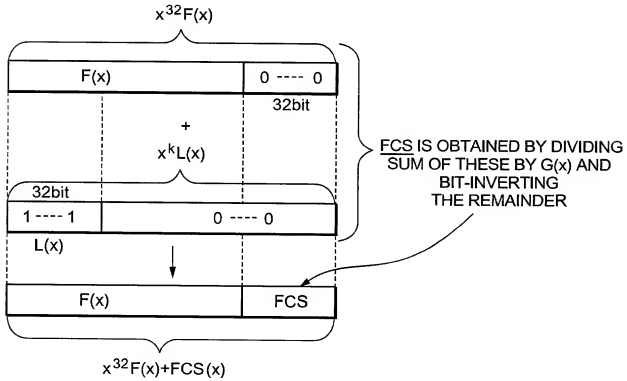


Fig.17

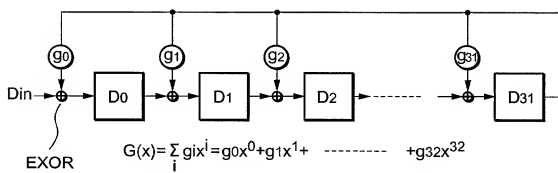


Fig.18

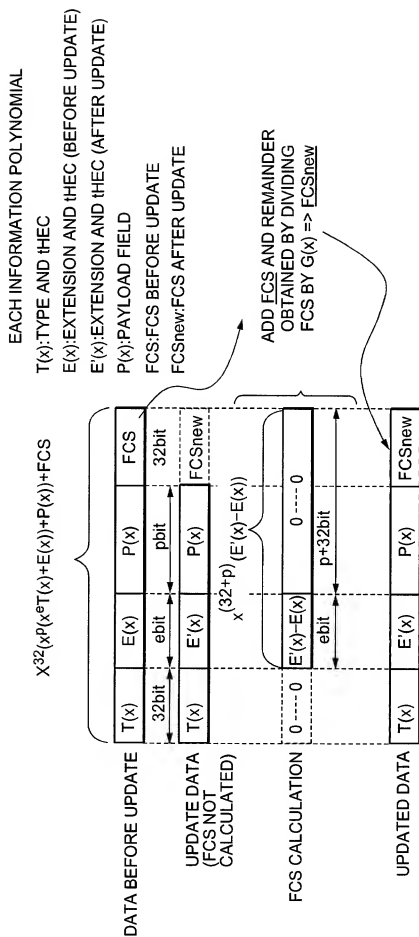


Fig.19

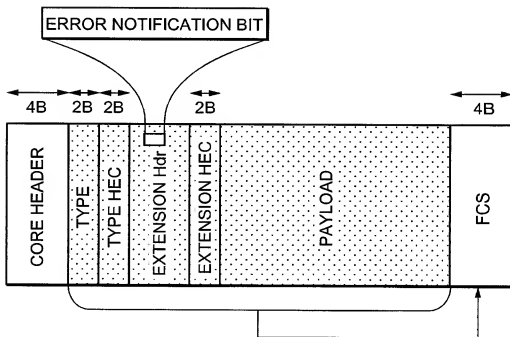


Fig.20

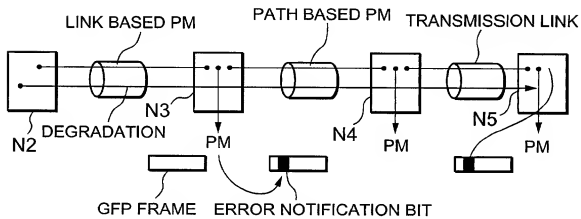


Fig.21